TRANSMITTAL LETTER (General - Patent Pending)	Docket No. END919970075US3

In Re Application Of: **Kresge et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
10/040,745	1/7/2002	Nguyen, Donghai D.	3729

Title: **ELECTRONIC PACKAGE FOR ELECTRONIC COMPONENTS AND METHOD OF MAKING THE SAME**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Reply Brief (14 pages)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kresge *et al.*

Examiner: Nguyen, Donghai D.

Serial No.: 10/040,745

Art Unit: 3729

Filed: 1/7/2002

For: **METHOD OF MAKING AN ELECTRONIC PACKAGE**

Commissioner for Patents
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REPLY BRIEF OF APPELLANTS

This Reply Brief addresses issues raised in the Examiner's Answer mailed dated December 16, 2003.

Issue 1

CLAIMS 80, 82-87, 91, AND 93-97 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §102(b) OVER US PATENT 4,882,454 TO PETERSON ET AL.

The Examiner rejected claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b) as allegedly being unpatentable over US Patent 4,882,454 to Peterson et al. Appellants present herein a Reply for claims 80, 87, and 91.

Claim 80

Appellants acknowledge that the Examiner's Answer is persuasive with respect to the following feature of claim 80: "positioning first and second pluralities of electrically conductive

members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate". Appellants agree with the Examiner's broad interpretation of the scope of the preceding feature of claim 80.

Appellants next present a Reply to the Examiner's Answer on two remaining issues relating to claim 80.

In a first issue relating to claim 80, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 80: "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate".

The Examiner's Answer states: "the thermally conductive layer being comprised of material having selected thickness and coefficient of thermal expansion (Col. 2, lines 19-21)". The Examiner further argues:

> "Col. 2, lines 40-53 of Peterson disclose the thermally conductive layer is optimized by proper choice of material, "coefficient of thermal expansion", and geometries, "selected thickness" to prevent the mismatch thermal expansion characteristics between printed wiring board and mounting devices (Col 1, lines 34-44). The mismatch thermal expansion characteristics between printed wiring board and mounting devices causes the solder connections between printed wiring board and mounting devices to fail. Therefore, preventing the mismatch of thermal expansion will prevent the failure of solder connections.... Appellants state that Peterson's disclosure is "non-specific"in col. 2, lines 44-49. However, Col. 2, lines 50-51 clearly states "These" (core modifications which are CTE and geometries, "thickness") involve the use of the materials or composite to made up the core. Therefore it is clearly or inherently identify the geometry and materials of the core, "thermally" conductive layer" is to be controlled. Furthermore, there is no positively statement in Peterson that precludes the geometries, "thickness" of the core from being

modified.... Examiner acknowledges that in Col. 2, lines 13-19 of Peterson disclose another advantage of his invention for having the elongated pads have a spring action that reduces the stress on the solder connections. As stated in Col. 1, lines 30-39, there are at least two methods to reduce mismatch between printed wiring and mounting components. One of the objects of Peterson's inventions is to have the printed wiring board, "multi-layer interconnection structure" that has the similar thermal expansion characteristics as mounting components, "semiconductor chip and circuitized substrate" and the other is the deflection of the printed wiring board. Therefore, optimizing the core by proper choice of material and geometries to have the similar thermal expansion as mounting components to promote reliability of solder connections is an invention of Peterson."

In Reply to the preceding argument by the Examiner, Appellants note that claim 80 claims a very specific parameter to be selected for substantially prevent failure of said solder connections. This specific parameter is: **thickness of the thermally conductive layer**. Peterson does not identify selecting the thickness of the thermally conductive layer for preventing failure of said solder connections. In fact, Peterson does not identify selecting the thickness of the thermally conductive layer for any purpose.

Applicants note that Peterson states on col. 2, lines 44-49: "Ideal performance in a surface mount application is achieved when CTE, thermal, weight and electrical properties are optimized by proper choice of materials and **geometries**. Core modifications can also be made to enhance thermal, CTE or weight properties when specific needs must be met" (emphasis added). The preceding non-specific statement by Peterson does not specifically identify the thickness of the thermally conductive layer for effectuating an optimization.

Since Peterson does not explicitly teach selecting the thickness of the thermally conductive layer for effectuating an optimization, the question is whether Peterson inherently teaches selecting the thickness of the thermally conductive layer for effectuating an optimization. Appellants contend that selecting the thickness of the thermally conductive layer for effectuating

an optimization is not inherently taught by Peterson. Appellants acknowledge that Peterson intends that the printed wiring board and surface mount components have similar thermal expansion characteristics as indicated in Peterson's stated object of the invention and as argued by the Examiner. However, said similarity of thermal expansion characteristics may be achieved in other way than through selecting the thickness of the thermally conductive layer for effectuating an optimization. Although Peterson states that the geometry of the core may be selected, Peterson does not identify any specific geometric property of the core. Appellants note that geometric properties of the core other than the thickness of the core may be selected to assist in achieving said similarity of thermal expansion characteristics. As example, one could select the core surface area, core volume, or core geometrical shape to assist in achieving said similarity of thermal expansion characteristics. Therefore it is not inherent in the Peterson disclosure to select the thickness of the core to assist in achieving said similarity of thermal expansion characteristics.

In addition, claim 80 is very specific as to claiming selecting the thickness and coefficient of thermal expansion **to substantially prevent failure of said solder connections**. Nowhere does Peterson explicitly disclose that it is an objective of Peterson's invention to prevent failure of the solder connections. The question is whether Peterson inherently discloses that it is an objective of Peterson's invention to prevent failure of the solder connections. Appellants contend that Peterson does not inherently disclose that it is an objective of Peterson's invention to prevent failure of the solder connections. Appellants acknowledge that Peterson discloses that the printed wiring board and surface mount components have similar thermal expansion characteristics as indicated in Peterson's stated object of the invention and as argued by the

Examiner. However, it is not inherent that one would attempt to have said similar thermal expansion characteristics for the purpose of preventing failure of the solder connections. For example, if the thermal expansion characteristics are mismatched, the printed wiring board and surface mount component may be subject to warpage and geometrical distortion during thermal transients without any failure in the solder connections occurring. Therefore, one might desire to achieve said similar thermal expansion characteristics for the purpose of reducing or eliminating said warpage and geometric distortion and not for the purpose of preventing failure of the solder connections. Therefore it is not inherent in the Peterson disclosure to select the thickness and coefficient of thermal expansion to substantially prevent failure of the solder connections.

As a further explanation of Appellants' preceding argument, Appellants contend that the Examiner's Answer has made the following erroneous statement to support the Examiner's argument: "The mismatch thermal expansion characteristics between printed wiring board and mounting devices causes the solder connections between printed wiring board and mounting devices to fail". The error in the preceding statement by the Examiner is that said mismatch in thermal expansion characteristics may cause said failure in solder connections, but does not necessarily cause said failure in solder connections. Whether failure occurs depends also on other factors such as: the degree of mismatch in thermal expansion characteristics and mechanical properties of the solder connections which control the ability of the solder connections to withstand the thermal stress caused by said mismatch in thermal expansion characteristics. The difference between "causes" and "may cause" is a key factor in resolving the inherency issue.

Accordingly, since Peterson does not explicitly or inherently teach the preceding feature of claim 80, Appellants maintain that Peterson does not anticipate claim 80. Accordingly, Appellants contend that the rejection of claim 80 is improper and should be reversed.

In a second issue relating to claim 80, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 80: "each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a **semiconductor chip** and a circuitized substrate" (emphasis added).

The Examiner's Answer asserted that "Appellants' argument that Peterson does not teach a semiconductor chip and solder connections adapted to be connected to a semiconductor chip, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure (IC packaging, "semiconductor chip", in col. l, lines 15-16; mounting pad, solder connection ", 103/104) is capable of performing the intended use (col. 2, lines 2-3), then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey,* 152 USPQ 235 (CCPA 1967) and *In re Oito,* 136 USPQ 458, 459 (CCPA 1963)."

In Reply to the preceding argument in the Examiner's Answer pertaining to said first issue relating to claim 80, Appellants contend that the Examiner is combing references, wherein Peterson's description of the Peterson invention is the primary references and Peterson's description of the prior art is a secondary reference. The Examiner is using Peterson's

description of the prior art to modify Peterson's description of the Peterson invention. Appellants assert that the Examiner is not permitted to combine references in a rejection under 35 U.S.C. §102(b). Therefore, Appellants maintain that is not anticipated by Peterson, since the Examiner relied on a combination of references rather than a single reference.

Moreover, the Examiner did not even offer an argument to support the combination of said references.

In addition, the Examiner's reliance on the Peterson's description of the prior art, as well as the Examiner's argument based on intended use, is a new ground of rejection which was not recited by the Examiner in the Office Action mailed April 23, 2003 and therefore cannot be used in the present Appeal. Indeed, the Examiner did not even address this feature of claim 80 (i.e., the semiconductor chip) in the Office Action mailed April 23, 2003. Therefore, Appellants contend that the Examiner has not satisfied the Examiner's burden of proof in relation to claim 80 and the rejection of claim 80 is per se improper. In essence, the Examiner has presented arguments relating to a semiconductor chip only in the Examiner's Answer and never presented any argument relating to the semiconductor chip in any office action.

In summary, the preceding arguments for said second issue relating to claim 80 demonstrate that Peterson does not anticipate claim 80, and the rejection of claim 80 under 35 U.S.C. §102(b) is improper and should be reversed.

Claim 87

Appellants acknowledge that the Examiner's Answer is persuasive with respect to the following feature of claim 87: "providing a first plurality of solder connections on said first plurality of electrically conductive members" in conjunction with "solder connections between said first plurality of electrically conductive members and said semiconductor chip". Appellants agree with the Examiner's broad interpretation of the scope of the preceding feature of claim 87.

Appellants next present a Reply to the Examiner's Answer on two remaining issues relating to claim 87.

In a first issue relating to claim 87, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 87: "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip". The Examiner's Answer with respect to this first issue relating to claim 87 is essentially the same as the Examiner's Answer with respect to the first issue relating to claim 80, discussed *supra*. Similarly, Appellants' Reply to the Examiner's Answer with respect to this first issue relating to claim 87 is essentially the same as Appellants' Reply to the Examiner's Answer with respect to the first issue relating to claim 80, discussed *supra*.

In a second issue relating to claim 87, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 87: "providing a **semiconductor chip** having a first surface including a plurality of contact sites thereon" (emphasis added). The Examiner's Answer with respect to this second issue relating to claim 87

is essentially the same as the Examiner's Answer with respect to the second issue relating to claim 80, discussed *supra*. Similarly, Appellants' Reply to the Examiner's Answer with respect to this second issue relating to claim 87 is essentially the same as Appellants' Reply to the Examiner's Answer with respect to the second issue relating to claim 80, discussed *supra*, except that the Examiner's "intended use" argument does not apply because claim 87 discloses an actual use, and not an intended use, of the semiconductor chip.

In summary, the preceding arguments for said second issue relating to claim 87 demonstrate that Peterson does not anticipate claim 87, and the rejection of claim 87 under 35 U.S.C. §102(b) is improper and should be reversed.

Claim 91

Appellants acknowledge that the Examiner's Answer is persuasive with respect to the following feature of claim 91: "each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip". Appellants agree with the Examiner's broad interpretation of the scope of the preceding feature of claim 91.

Appellants next present a Reply to the Examiner's Answer on three remaining issues relating to claim 91.

In a first issue relating to claim 91, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 91: "said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first

plurality of electrically conductive members and said semiconductor chip". The Examiner's Answer with respect to this first issue relating to claim 91 is essentially the same as the Examiner's Answer with respect to the first issue relating to claim 80, discussed *supra*. Similarly, Appellants' Reply to the Examiner's Answer with respect to this first issue relating to claim 91 is essentially the same as Appellants' Reply to the Examiner's Answer with respect to the first issue relating to claim 80, discussed *supra*.

In a second issue relating to claim 91, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 91: "each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a **semiconductor chip**" (emphasis added)" (emphasis added). The Examiner's Answer with respect to this second issue relating to claim 91 is essentially the same as the Examiner's Answer with respect to the second issue relating to claim 80, discussed *supra*. Similarly, Appellants' Reply to the Examiner's Answer with respect to this second issue relating to claim 91 is essentially the same as Appellants' Reply to the Examiner's Answer with respect to the second issue relating to claim 80, discussed *supra*.

In a third issue relating to claim 91, the Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 91: "positioning a second electrically conductive layer between said first electrically conductive layer and said thermally conductive layer wherein said second electrically conductive layer comprises a **first plurality of shielded signal conductors**" (emphasis added)". The Examiner's Answer has provided an argument relating to the preceding third issue relating to claim 91. However, the Examiner's argument in the Examiner's Answer is a new ground of rejection which cannot be used in the

present Appeal, since the Examiner did not present any argument relating to the shielded signal conductors in any office action. Accordingly, Appellants contend that the Examiner has not satisfied the Examiner's burden of proof in relation to claim 91 with respect to said third issue.

Issue 2

CLAIMS 81, 88, AND 92 ARE NOT UNPATENTABLE UNDER 35 U.S.C. §103(a) OVER PETERSON ET AL.

The Examiner rejected claims 81, 88, and 92 under 35 U.S.C. §103(a) as allegedly being unpatentable over Peterson et al. Appellants present herein a Reply for claims 81 and 92.

Claim 81

The Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 81: "wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F".

The Examiner's Answer argues: "Regarding claims 81 and 92, Peterson et al. disclose the step of laminating except for the specific range of temperature and pressure. At the time the invention was made it would have been obvious matter of design choice to one having ordinary skill in the art to specify a specific range of temperature and pressure in the step of lamination because Applicant have not disclose that the specific temperature and pressure provide an

advantage, are used for a particular purpose, or solve a stated problem. One ordinary skin in the art would have expected Applicants' invention to perform equally well as Peterson et al.'s invention. Therefore, it would have been obvious matter of design choice to specify a specific range of temperature and pressure in the step of laminating the first and second dielectric layers onto the thermally conductive layer to obtain the invention as specified in claims 81 and 92."

The Examiner's Answer further argues: "Appellants argue that the Examiner has not demonstrated that one having ordinary skill in the art would laminate the first and second dielectric layers onto the thermally conductive layer at pressure of from about 1000 to 1500 psi and at a temperature of from 600 to about 750 degrees Celsius. Peterson's col. 2, lines 62-63 disclose the first and second dielectric layers laminates onto the thermally conductive layer. This laminating step to form the printed circuit board is must perform at certain range of pressure and temperature, which may include the pressure and temperature ranges. There is no limitation in the claim or specification that precludes the use different pressure and temperature in the process of laminating the first and second dielectric layer onto the thermally conductive layer."

In response to the preceding argument in the Examiner's Answer, Appellants contend that the Examiner's argument is not persuasive, because the Examiner has not demonstrated that one of ordinary skill in the art would, as a matter of design choice, laminate at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F. Design choice is literally a "choice" and different designers would **choose** different ranges of pressure and temperature. The Examiner has not supplied any evidence that the designer would choose a pressure of from about 1000 to about 1500 psi and a temperature of from about 600 to about 750 ° F.

In order to establish a *prima facia* case of obviousness, the Examiner must supply an additional reference(s) evidencing performance of said laminating at a pressure and temperature in the ranges recited in claim 81, which the Examiner has not done. If the Examiner's argument were persuasive, no Examiner would ever have to supply a reference that discloses a claimed operating range.

Accordingly, Appellants contend that the Examiner has not established a *prima facie* case of obviousness in relation to claim 81.

Claim 92

The Examiner's Answer responded to Appellants' assertion that Peterson does not teach the following feature of claim 92: "wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 1500 psi and at a temperature of from about 600 to about 750 ° F".

The Examiner's Answer with respect to the preceding feature of claim 92 is essentially the same as the Examiner's Answer with respect to the essentially same feature of claim 81, discussed *supra*. Similarly, Appellants' Reply to the Examiner's Answer with respect to the preceding feature of claim 92 is essentially the same as Appellants' Reply to the Examiner's Answer with the essentially same feature of claim 81, discussed *supra*.

SUMMARY

In summary, Appellants respectfully request reversal in the office action of April 23, 2003 of: the rejection of claims 80, 82-87, 91, and 93-97 under 35 U.S.C. §102(b); and the rejection of claims 81, 88-90, and 92 under 35 U.S.C. §103(a)

Respectfully submitted,

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